inputting a first gate voltage and a [periodically changing] second gate voltage; the first gate voltage having a voltage level that turns on the switching transistor and the second gate voltage having a voltage level that turns off the switching transistor

supplying the first gate voltage and the second gate voltage, selectively via a switching device, to the gate [line] lines, said switching device being controlled by the shift register, wherein the first gate voltage varies before the second gate voltage is supplied to the gate lines[; and

supplying the first voltage, via the switching device, to the gate line, said switching device being controlled by the shift register, wherein a minimum value of the second voltage is higher than a maximum value of the first voltage].

a1 cmdd

8. (Amended) The method as claimed in claim 7, wherein the first gate voltage is supplied to the gate [line] lines during a time interval when the thin film transistors connected to the gate lines are turned on.

REMARKS

The Applicant has amended claims 1-8. Accordingly, claims 1-9 remain pending in the application.

35 U.S.C. § 102

The Examiner has rejected claims 1 and 7-9 under 35 U.S.C. § 102(e) as anticipated by Tomita. Applicant respectfully traverses that rejection for at least the following reasons.

The Examiner has stated that Tomita shows:

"*a plurality of gate line 103 (figure 1, column 6, lines 39-43) as read on the claims. A storage capacitor line driving circuit 109 connects to the plurality of scanning line driving circuit 103 (figure 10), a scanning line driving circuit 103 receiving first direct current voltage generating circuit 701 and second direct current voltage generating circuit 703 and outputting first voltage 705 and second voltage 707 to drive the gate signal lines sequentially . . .* ."

Insofar as Applicant can understand this rejection, Applicant respectfully submits that the Examiner is mistaken about Tomita, and in any event, Applicant submits that Tomita does not disclose the claimed invention.

At the outset, the Examiner states that "*storage capacitor line driving circuit 109 connects to the plurality of scanning line driving circuit 103 (figure 10).*" Applicant does not see any such plurality of scanning line driving circuits, only a single line driving circuit 103.

More importantly, the Examiner also states that "*a scanning line driving circuit 103 receiv[es] first direct current voltage generating circuit 701 and second direct current voltage generating circuit 703 and output[s] first voltage 705 and second voltage 707 to drive the gate signal lines sequentially.*" Figure 9 clearly shows that the first and second voltage generating circuits 701 and 703 and the switches $S_1 \ldots S_n$ all belong to the storage capacitor line driving circuit 109 and **not** to the scanning (i.e. gate) line driving circuit 103. The storage capacitor line driving circuit 109 drives the storage capacitor lines 143, **not** the scanning lines 125! Nor do the output signal lines 143, labeled $H_1 \ldots H_n$, drive the gates 129 or scanning lines 125 of the TFTs.

Thus, in summary, Tomita discloses a device where first and second voltages are selected to be applied to *storage capacitor lines* 143 by a storage capacitor line driving circuit 109, and **not** to the gate signal lines of the TFTs by a gate driving circuit.

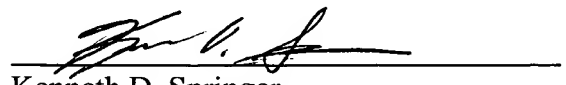
On the other hand, in the invention of claims 1 and 7, a *gate* driver is connected to the plurality of the *gate* signal lines, the *gate* driver receiving first *gate* and second *gate* voltages and outputs one of the first gate and second *gate* voltages in such a manner to drive the *gate signal lines* for the gates of the TFTs. Therefore, Tomita does not disclose a device or method according to the present claimed invention. Accordingly, Applicant respectfully submits that claims 1 and 7-9 are allowable over the cited art and respectfully requests that the Examiner withdraw his rejection of these claims. Claims 2-6 and 8, dependent from claims 1 and 7 respectively are deemed to be similarly allowable.

In view of the foregoing, Applicants respectfully request that the application be reconsidered, that claims 1-9 be allowed, and the application pass to issue. Please charge any insufficiency or credit any overpayment to Deposit Account No. 50-0911.

Respectfully submitted,

LONG ALDRIDGE & NORMAN, LLP

Date: 14 November 2000



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